



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,284	09/24/2003	Mitsunori Sakama	0553-0185.01	6594
7590 Edward D. Manzo Cook, Alex, McFarron, Manzo, Cummings & Mehler, Ltd. 200 West Adams St., Ste. 2850 Chicago, IL 60606			EXAMINER MONDT, JOHANNES P	
			ART UNIT 3663	PAPER NUMBER
			MAIL DATE 11/26/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/669,284	Applicant(s) SAKAMA ET AL.	
	Examiner Johannes P. Mondt	Art Unit 3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2007 and 11 September 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 41-71 is/are pending in the application.
- 4a) Of the above claim(s) 51-56, 60, 61, 65, 66, 70 and 71 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 41-50, 57-59, 62-64 and 67-69 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### DETAILED ACTION

Response to Notice of Non-Responsive Amendment filed 9/11/07 in conjunction with previously submitted Response filed 4/27/07 on a request for Information under 37 C.F.R. 1.105 and response in traverse of rejections in the office action mailed 12/27/06 form the basis for this Office Action. Comments on said Responses are included below under "Response to Arguments".

#### *Specification*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The Specification and Abstract are objected to because the lower limits of hydrogen and nitrogen and disclosed (see [0015] in the published application or page 4, lines 22-29 in the original Specification as filed; see also Abstract) are not enabled by applicants' experimental data (see Experimental results 1 and 2 in Response filed 9/11/07).

#### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. **Claims 41-50, 57-59, 62-64 and 67-69** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable

one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, response to 37 C.F.R. 105 in the form of provided Experimental Results 1 and 2 show clearly that the lower limits of the hydrogen concentration and the nitrogen concentration as measured by applicants are more than one order of magnitude higher than the lower limits of the same as claimed (see all independent claims). Therefore, the claimed ranges for the nitrogen and hydrogen concentrations are not enabled, with reference to the MPEP 2164.08, first paragraph.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. ***Claims 41, 44, 45, 48, 51, 54, 57-61 and 67-69*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al (5,804,878) (previously cited) in view of Yamazaki et al (JP408055847A) (as made of record in IDS and previously cited), for which Yamazaki et al (5,970,384) (also made of record in IDS), - of which JP408055847A is Foreign Priority, serves as translation, and Wörhoff et al (IEEE Catalog Nr. 0-7803-4947 (04/1998): "Silicon oxynitride in integrated optics", in LEOS'98, Volume 2, pp. 370-371 (1998)).

*On claim 41: Miyazaki et al teach a semiconductor device comprising a pixel portion and a driver circuit on a substrate (cf. col. 10, l. 52-col. 11, l. 3; Figures 1 and 6), comprising:*

*a base film 2 (corresponding to element with numeral 2 in Figure 1, and visible in Figure 6);*

*first, second and third semiconductor layers over said base film (said semiconductor layers corresponding to element with numeral 5 (obtained from semiconductor film 3) in Figure 1 (col. 7, l. 16-19) and corresponding to the semiconductor layers underneath each of three thin film transistors (pixel transistor TFT3 and driver transistors TFT1, TFT2, respectively, in Figure 6);*

*a first gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent to said first semiconductor layer with a gate insulating film 6 (cf. col. 7, l. 16-18) interposed therebetween, wherein a first LDD region (corresponding to region 209 or 210 in Figure 2; col. 9, l. 30-38) in said first semiconductor layer (of TFT3) is not overlapped with said first gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that film 507 (207) is used as mask; col. 9, l. 30-38);*

*a second gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said second semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a second LDD region in said semiconductor layer (of TFT2) is overlapped with said second gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 506 is used as mask; col. 9, l. 30-38);*

a third gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said third semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a third LDD region in said semiconductor layer (of TFT3) is overlapped with said third gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 505 is used as mask; col. 9, l. 30-38); and

wherein said pixel portion comprises said first semiconductor "film" (actually: layer: see under "Objections to Claims"), and said driver portion comprises said second and third semiconductor "films" ( actually: layers: see under "Objections to Claims") (cf. col. 10, l. 52-61).

*Miyazaki et al* do not necessarily teach the limitation defined in the final five lines of claim 41: i.e.,

(a) "each of said gate insulating films and said base film comprises hydrogenated silicon oxynitride, and contains oxygen, nitrogen and hydrogen and contains oxygen, nitrogen and hydrogen, wherein the concentration of oxygen and nitrogen of said hydrogenated silicon oxynitride film are from 55 to 70 at% and from 0.1 to 6 at%, respectively; and

(b) wherein the hydrogen concentration of said hydrogenated silicon oxynitride film is from 0.1 to 3 at%.

*However, it would have been obvious* to include said limitation (a) in view of *Yamazaki et al*, who, in a patent on an improved composition of gate insulation films in thin film transistors, - hence closely related art, teach the selection of hydrogenated silicon oxynitride of which the hydrogenation is reduced (cf. abstract): starting from a

silicon dioxide film (concentration thus being  $2/3 = 66.7\%$  oxygen, thus falling well within the claimed range of 55 to 70 percent) wherein through annealing by  $\text{NH}_3$  nitrogen bonds are created so as to reduce the number of un-paired bonds (col. 4, l. 1-60) and in particular replacing the deleterious Si-H bonds and Si-OH bonds through replacement of the a substantial portion of the hydrogen with nitrogen (cf. col. 7, l. 1-32), with a stated nitrogen concentration of typically between 0.1 and 6 atomic % of N (col. 11, l. 49-54), thus substantially overlapping the claim limitation of 0.1 to 6 atomic % of N. Because the nitrogen only is able to replace pre-existing hydrogen and the hydrogen is further reduced through an annealing step (cf. abstract) it can be concluded logically that the H concentration is substantially less than 6 atomic %. Please note that Yamazaki et al teach the above film for both a gate insulating film (col. 3, l. 5-10) and for replacing a silicon oxide film "on an active layer", which does apply to both gate and base films in Miyazaki et al.

*Motivation* to include the teaching by Yamazaki et al in the invention by Miyazaki et al at least derives from the resulting improvement of the gate insulation film's insulating properties through the substantial reduction of single hydrogen bonds.

*Furthermore, it would have been obvious to include limitation ad (b) on hydrogen concentration in view of Wörhoff et al, who, in a publication on the "state of the art" of silicon oxynitride deposition" with application to integrated circuits (See Title and Abstract), hence analogous and pertinent to Yamazaki et al, teach that the H concentration in silicon oxynitride films manufactured by plasma enhanced or low pressure CVD, the methods employed by Yamazaki et al, do contain hydrogen in the*

claimed range, i.e., plasma-enhanced CVD or LCVD, the methods used by Yamazaki et al as cited for the hydrogen content (col. 5, l. 45-59), followed by an anneal step as also taught by Yamazaki et al (see col. 7, l. 1-32 as cited) in an effort to reduce said hydrogen content leads to a hydrogen content in a range that includes 0.4 at%, and 1.3 at% and 4.5%, thus quite substantially overlapping with the range as claimed (01.- 3 at%) (see Table 2 and discussion, especially section II (page 370, second column). It thus appears that the overall hydrogen content of the hydrogenated oxynitride film is characterized by a hydrogen concentration in the claimed range when made in a same manner as carried out by Yamazaki et al as documented by the measurements published by Wörhoff et al.

Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

*On claim 44:* said substrate is a glass substrate (cf. col. 8, l. 27-35).

*On claim 45:* Miyazaki et al teach a semiconductor device comprising a pixel portion and a driver circuit on a substrate (corresponding with element 201 in Figure 1) (cf. col. 8, l. 28-36, 10, l. 52-col. 11, l. 3; Figures 1 and 6), comprising:

first, second and third semiconductor layers over said substrate (said semiconductor layers corresponding to element with numeral 5 in Figure 1 (col. 7, l. 16-19) and corresponding to the semiconductor layers underneath each of three thin film



transistors (pixel transistor TFT3 and driver transistors TFT1, TFT2, respectively, in Figure 6);

a first gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent to (claim 45) or over (claim 51) (N.B.: "adjacent" means "nearby", "over" means "across a barrier or intervening space" (see Merriam-Webster's Collegiate Dictionary, 10<sup>th</sup> Edition, pages 14 and 827, respectively), while it is inherent to any gate electrode in an insulated gate field effect transistor such as the disclosed TFT to be both nearby and across a barrier from said semiconductor layer, the latter being the channel region of the insulated gate field effect transistor), said first semiconductor layer with a gate insulating film 6 (cf. col. 7, l. 16-18) interposed therebetween, wherein a first LDD region (corresponding to region 209 or 210 in Figure 2; col. 9, l. 30-38) in said first semiconductor layer (of TFT3) is not overlapped with said first gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that film 507 (207) is used as mask; col. 9, l. 30-38);

a second gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said second semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a second LDD region in said semiconductor layer (of TFT2) is overlapped with said second gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 506 is used as mask; col. 9, l. 30-38);

wherein said pixel portion comprises said first semiconductor "film" (actually: layer: see under "Objections to Claims"), and said driver portion comprises said second and third semiconductor "films" ( actually: layers: see under "Objections to Claims") (cf. col. 10, l. 52-61).

*Miyazaki et al* do not necessarily teach the limitation defined in the final five lines of claim 41: i.e.,

(a) "each of said gate insulating films and said base film comprises hydrogenated silicon oxynitride, and contains oxygen, nitrogen and hydrogen and contains oxygen, nitrogen and hydrogen, wherein the concentration of oxygen and nitrogen of said hydrogenated silicon oxynitride film are from 55 to 70 at% and from 0.1 to 6 at%, respectively; and

(b) wherein the hydrogen concentration of said hydrogenated silicon oxynitride film is from 0.1 to 3 at%.

*However, it would have been obvious* to include said limitation (a) in view of *Yamazaki et al*, who, in a patent on an improved composition of gate insulation films in thin film transistors, - hence closely related art, teach the selection of hydrogenated silicon oxynitride of which the hydrogenation is reduced (cf. abstract): starting from a silicon dioxide film (concentration thus being  $2/3 = 66.7\%$  oxygen, thus falling well within the claimed range of 55 to 70 percent) wherein through annealing by  $\text{NH}_3$  nitrogen bonds are created so as to reduce the number of un-paired bonds (col. 4, l. 1-60) and in particular replacing the deleterious Si-H bonds and Si-OH bonds through replacement of the a substantial portion of the hydrogen with nitrogen (cf. col. 7, l. 1-32), with a stated nitrogen concentration of typically between 0.1 and 6 atomic % of N (col. 11, l. 49-54), thus substantially overlapping the claim limitation of 0.1 to 6 atomic % of N. Because the nitrogen only is able to replace pre-existing hydrogen and the hydrogen is further reduced through an annealing step (cf. abstract) it can be concluded logically

that the H concentration is substantially less than 6 atomic %. Please note that Yamazaki et al teach the above film for both a gate insulating film (col. 3, l. 5-10) and for replacing a silicon oxide film "on an active layer", which does apply to both gate and base films in Miyazaki et al.

*Motivation* to include the teaching by Yamazaki et al in the invention by Miyazaki et al at least derives from the resulting improvement of the gate insulation film's insulating properties through the substantial reduction of single hydrogen bonds.

*Furthermore, it would have been obvious to include limitation ad (b) on hydrogen concentration in view of Wörhoff et al*, who, in a publication on the "state of the art" of silicon oxynitride deposition" with application to integrated circuits (See Title and Abstract), hence analogous and pertinent to Yamazaki et al, teach that the H concentration in silicon oxynitride films manufactured by plasma enhanced or low pressure CVD, the methods employed by Yamazaki et al, do contain hydrogen in the claimed range, i.e., plasma-enhanced CVD or LCVD, the methods used by Yamazaki et al as cited for the hydrogen content (col. 5, l. 45-59), followed by an anneal step as also taught by Yamazaki et al (see col. 7, l. 1-32 as cited) in an effort to reduce said hydrogen content leads to a hydrogen content in a range that includes 0.4 at%, and 1.3 at% and 4.5%, thus quite substantially overlapping with the range as claimed (0.1-3 at%). It thus appears that the overall hydrogen content of the hydrogenated oxynitride film is characterized by a hydrogen concentration in the claimed range when made in a same manner as carried out by Yamazaki et al as documented by the measurements published by Wörhoff et al.

Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 48: Miyazaki et al teach a semiconductor device comprising a pixel portion and a driver circuit on a substrate (corresponding with element 201 in Figure 1) (cf. col. 8, l. 28-36, 10, l. 52-col. 11, l. 3; Figures 1 and 6), comprising:

first, second and third semiconductor layers over said substrate (said semiconductor layers corresponding to element with numeral 5 in Figure 1 (col. 7, l. 16-19) and corresponding to the semiconductor layers underneath each of three thin film transistors (pixel transistor TFT3 and driver transistors TFT1, TFT2, respectively, in Figure 6);

a first gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent to (claim 48) or over (claim 54) said first semiconductor layer with a gate insulating film 6 (cf. col. 7, l. 16-18) interposed therebetween (N.B.: "adjacent" means "nearby", "over" means "across a barrier or intervening space" (Merriam-Webster's Collegiate Dictionary, 10<sup>th</sup> Edition, pages 14 and 827, respectively), while it is inherent to any gate electrode in an insulated gate field effect transistor such as the disclosed TFT to be both nearby and across a barrier from said semiconductor layer, the latter being the channel region of the insulated gate field effect transistor), wherein a first LDD region (corresponding to region 209 or 210 in Figure 2; col. 9, l. 30-38) in said first

semiconductor layer (of TFT3) is not overlapped with said first gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that film 507 (207) is used as mask; col. 9, l. 30-38);

a second gate electrode (corresponding to 7 in Figure 1; col. 7, l. 20-21; cf. Figure 6) adjacent said second semiconductor layer with said gate insulation film 6 (cf. col. 11, l. 13-18) therebetween, a second LDD region in said semiconductor layer (of TFT2) is overlapped with said second gate electrode (cf. Figure 6 and col. 10, l. 60-64: note that the anode oxide film 506 is used as mask; col. 9, l. 30-38);

wherein said pixel portion comprises said first semiconductor "film" (actually: layer: see under "Objections to Claims"), and said driver portion comprises said second and third semiconductor "films" ( actually: layers: see under "Objections to Claims") (cf. col. 10, l. 52-61).

*Miyazaki et al* do not necessarily teach the limitation defined in the final five lines of claim 41: i.e.,

(a) "each of said gate insulating films and said base film comprises hydrogenated silicon oxynitride, and contains oxygen, nitrogen and hydrogen and contains oxygen, nitrogen and hydrogen, wherein the concentration of oxygen and nitrogen of said hydrogenated silicon oxynitride film are from 55 to 70 at% and from 0.1 to 6 at%, respectively; and

(b) wherein the hydrogen concentration of said hydrogenated silicon oxynitride film is from 0.1 to 3 at%.

*However, it would have been obvious* to include said limitation (a) in view of *Yamazaki et al*, who, in a patent on an improved composition of gate insulation films in

thin film transistors, - hence closely related art, teach the selection of hydrogenated silicon oxynitride of which the hydrogenation is reduced (cf. abstract): starting from a silicon dioxide film (concentration thus being  $2/3 = 66.7\%$  oxygen, thus falling well within the claimed range of 55 to 70 percent) wherein through annealing by  $\text{NH}_3$  nitrogen bonds are created so as to reduce the number of un-paired bonds (col. 4, l. 1-60) and in particular replacing the deleterious Si-H bonds and Si-OH bonds through replacement of the a substantial portion of the hydrogen with nitrogen (cf. col. 7, l. 1-32), with a stated nitrogen concentration of typically between 0.1 and 6 atomic % of N (col. 11, l. 49-54), thus substantially overlapping the claim limitation of 0.1 to 6 atomic % of N. Because the nitrogen only is able to replace pre-existing hydrogen and the hydrogen is further reduced through an annealing step (cf. abstract) it can be concluded logically that the H concentration is substantially less than 6 atomic %. Please note that Yamazaki et al teach the above film for both a gate insulating film (col. 3, l. 5-10) and for replacing a silicon oxide film "on an active layer", which does apply to both gate and base films in Miyazaki et al.

*Motivation* to include the teaching by Yamazaki et al in the invention by Miyazaki et al at least derives from the resulting improvement of the gate insulation film's insulating properties through the substantial reduction of single hydrogen bonds.

*Furthermore, it would have been obvious to include limitation ad (b) on hydrogen concentration in view of Wörhoff et al, who, in a publication on the "state of the art" of silicon oxynitride deposition" with application to integrated circuits (See Title and Abstract), hence analogous and pertinent to Yamazaki et al, teach that the H*

concentration in silicon oxynitride films manufactured by plasma enhanced or low pressure CVD, the methods employed by Yamazaki et al, do contain hydrogen in the claimed range, i.e., plasma-enhanced CVD or LCVD, the methods used by Yamazaki et al as cited for the hydrogen content (col. 5, l. 45-59), followed by an anneal step as also taught by Yamazaki et al (see col. 7, l. 1-32 as cited) in an effort to reduce said hydrogen content leads to a hydrogen content in a range that includes 0.4 at%, and 1.3 at% and 4.5%, thus quite substantially overlapping with the range as claimed (01.- 3 at%). It thus appears that the overall hydrogen content of the hydrogenated oxynitride film is characterized by a hydrogen concentration in the claimed range when made in a same manner as carried out by Yamazaki et al as documented by the measurements published by Wörhoff et al.

Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

*On claims 57, 58 and 59:* said second semiconductor layer comprises a second source region and a second drain region (doped regions 208 and 211, see Figures 1, 6 and 7) (col. 7, 30-38, and elements 8; cf. col. 11, l. 13-18), and a second channel region between said second source and second drain regions (see claim 23 in Miyazaki et al; furthermore, a channel between source and drain is utterly inherent to any field effect transistor), said second LDD region is between said second channel and drain regions

(element 209 is in between the channel, as the remaining portion after source/drain implementation of semiconductor region 203, and source/drain regions 208/211; cf. Figure 1), and said second source region is in (electrical) contact with said channel region (alternatively, said second source region can well be defined as comprising the LDD region on its side, in which alternative rejection the contact is not merely electrical but also material).

*On claims 67- 69:* the interlayer insulating film also is an insulating film on an active layer, namely on the gate electrode, and hence the teaching by Yamazaki et al also applies to said interlayer insulating film (col. 4, l. 48-59).

**2a. Claims 42, 46 and 49** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al, Yamazaki et al and Wörhoff et al as applied to claims 41 and 45, respectively, above, and further in view of Patent Document owned by Sharp KK (Publication No.: JP 11101974 A) (previously cited). As detailed above, claims 41, 45, 48, 51, 54 are unpatentable over Miyazaki et al in view of Yamazaki et al. *Neither necessarily teach* the further limitation as defined by claims 42, 46, 49, 52, 55, respectively. *However, it would have been obvious* to include said further limitation in view of the Patent Document by Sharp KK, who teaches the application of liquid crystal display devices based on TFT transistors to (see Use): personal computers, portable information terminals, video apparatus, inter alia. Said application are thus seen to be obvious applications of the invention obtained by combining Miyazaki et al and Yamazaki et al.



3. **Claims 43, 47 and 50** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al , Yamazaki et al and Wörhoff et al as applied to claims 41, 45, 48, 51, 55, respectively, above, and further in view of Tang et al (5,684,365)(previously cited). *As detailed above, claims 41, 45 and 48 are unpatentable over Miyazaki et al in view of Yamazaki et al. Neither necessarily teach the further limitation defined by claims 43, 47, 50, 53 and 56, respectively. However, it would have been obvious to include said further limitation in view of Tang et al, who, in a patent on a electroluminescence (EL) display teach the inclusion of TFT electroluminescent pixels for the specific purpose to eliminate the need to pattern the EL cathode, from which it follows that the invention by Miyazaki et al finds obvious applications to EL display devices. Motivation thus stems from the immediate and obvious applicability of the invention by Miyazaki et al to the field of EL display technology.*

4. **Claim 62-64** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazaki et al, Yamazaki et al and Wörhoff et al as applied to claim 41 above, and further in view of Yamazaki et al (5,784,073) (previously cited), henceforth referred to as Yamazaki2. *As detailed above, claims 41, 45 and 48 are unpatentable over Miyazaki et al in view of Yamazaki et al.*

*Furthermore, Miyazaki et al teach that said semiconductor device further comprises:*

*a first insulating film 207 (cf. Figure 7 and col. 9, l. 16-30) over said first, second, and third gate electrodes;*

a second insulating film 217 (cf. Figure 7 and col. 10, l. 30-35) over said first insulating film;

and

a pixel electrode 13, 508 (cf. Figures 1 and 7) (cf. col. 8, l. 7-25 and col. 10, l. 63 – col. 11, l. 1) over said second insulating film connected to said first semiconductor layer (i./e, the layer of the pixel TFT: this is what makes said TFT3 a pixel TFT, being inherent in the pixel TFT3).

*Neither Miyazaki et al nor Yamazaki et al necessarily teach the further limitation as defined by claims 62-66, namely: of a third insulation film comprising organic resin over said second insulating film, with said pixel electrode also being over said third insulating film.*

*However, it would have been obvious to include said further limitation in view of Yamazaki2, who, in a patent on an electro-optical device based on thin film transistors (col. 3, l. 33 – col. 4, l. 25), - hence closely related to the invention by Miyazaki et al, teach the inclusion of an organic resin layer 119 for the specific purpose of flattening prior to forming the pixel electrode thereon (cf. col. 16, l. 16-35).*

*Motivation, to include the teaching by Yamazaki2 in the invention by Miyazaki et al, lies in the resulting substantially flat surface over which the pixel electrode can be laid, thus reducing the abrasiveness, and with it the mechanical vulnerability, of the structure. Furthermore, the mechanical contact between the pixel electrode and the insulating material is enhanced through the planarization, thus increasing mechanical integrity.*

***Response to Arguments***

1. Applicant's arguments filed 9/11/07 and 4/27/07 have been fully considered but they are not persuasive. In particular, the experimental results 1 and 2 do not constitute evidence of reduction to practice of the lower limits of the concentrations of nitrogen and hydrogen which was examiner's main concern (see page 3). On the contrary: both Experimental Results 1 and 2 show hydrogen concentrations and nitrogen concentrations of more than one order of magnitude above the lower limits of 0.1 atomic% (see tables in said Response to Notice of Non-Responsive Amendment for Experimental results 1 and 2, and compare the latter with the ranges for the nitrogen and hydrogen concentrations in independent claims 41, 45, 48 (and dependent claims 67-69).. Applicant is referred to MPEP 2164.08, first paragraph, especially as it relates to range limitations. Therefore, it is concluded that the invention as claimed is not enabled. See the above rejection under 35 U.S.C. 112, first paragraph.

With regard to the traverse of the rejections, counter to applicants' argument (4/27/07 Response, pages 2-5) and allegation that in Yamazaki (JP 08-55847 or US 5,970,384) H<sub>2</sub> (i.e., hydrogen) is not included as a raw material, applicants are respectfully referred to col. 3, l. 41-55 on their method of improving the silicon oxide film, in which they state that:

The first invention is characterized by the fact that a silicon oxide film is improved so as to be satisfactory for use as a gate insulating film by heat treating a silicon oxide film, which has been formed by a PVD method or a CVD method, in an N.sub.2 O atmosphere at 300-700.degree. C., and preferably at 500-600.degree. C., and irradiating with ultraviolet light at the same time. Heat treatment at 300-700.degree. C., and

preferably at 500-600.degree. C. in a hydrogen atmosphere, or hydrogen nitride atmosphere such as an ammonia (NH.sub.3) or hydrazine (N.sub.2 H.sub.4) atmosphere, may be carried out prior to the abovementioned heat treatment/ultraviolet light irradiation process. Furthermore, irradiation with ultraviolet light in the same way as in the N.sub.2 O atmosphere may be carried out in the heating process in a hydrogen or hydrogen nitride atmosphere.

Here, bold font was added for emphasis as it shows that Yamazaki et al do include hydrogen as raw material gas. Wörhoff only confirms that efforts to reduce the hydrogen content along the methods by applicant and Yamazaki et al result in a range commensurate with Yamazaki et al, and, from Experimental Results 1 and 2, commensurate with what applicants in effect have found. Therefore, said argument fails to persuade and the previous rejections are made to stand.

### ***Conclusion***

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Application/Control Number:  
10/669,284  
Art Unit: 3663

Page 20

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM  
November 24, 2007

Primary Examiner:

  
Johannes Mondt (Art Unit: 3663)